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Education Society's Group of Institutions - Integrated Campus
(UGC AUTONOMOUS INSTITUTION)

EAMCET/ECET/ICET/PGECET Code NNRG

Department of Electronics and Communication Engineering

A Report on One Week Student Development Program

"Advanced VLSI Design: RTL to GDS II"

(16th - 21st October 2023)

Department of Electronics and Communication Engineering in association with IETE Student Forum (ISF) has successfully organized a one week Student Development Program (SDP) on "Advanced VLSI Design: RTL to GDS II" for IV B.Tech students from 16th to 21st October 2023. The objective of this student development program is to provide the insights and get expertise on advanced design and verification EDA tools. The SDP focused mainly on the design, implementation and verification of Digital VLSI Logics using Verilog HDLs and the use of Advanced IP cores for design. Further, a hands-on session on physical layout design, implementation and verification using backend EDA tools was demonstrated.

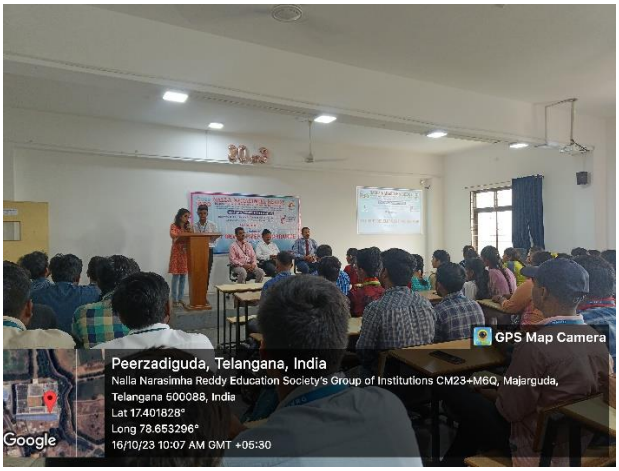
The final year students will have an exposure to advanced Artix-7 FPGA, Zynq-7000 SoC, Xilinx Vivado ML Enterprise tool for design, verification and Synthesis. After completion of student development program, the students will be able to design, verify, synthesize, simulate and realize the digital logics using IP Cores and advanced FPGAs.

Total 42 students were registered for the student development program and participation certificate for all 42 were issued by the institute.

Dr. B. HariPrasad Naik, **Ms. N.Lavanya** and **Mr. K. Ramesh,** worked as Faculty coordinators for the one week student development program.

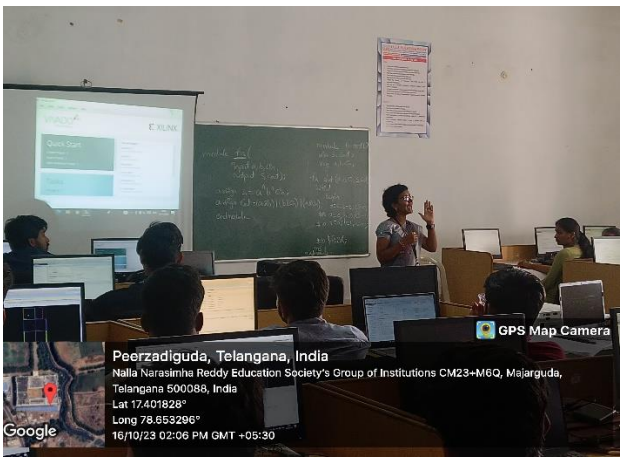
Day-1

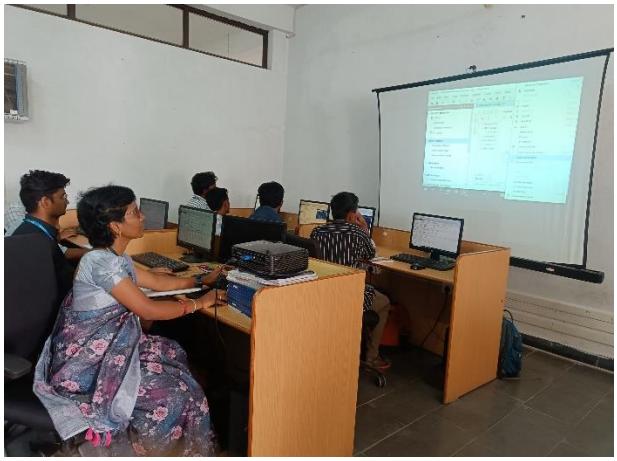
The workshop was inaugurated by the Director of the Institute, Dean School of Engineering and Head of the Department, ECE at 10 am.



In the morning session, Dr.C.V.Krishna Reddy, delivered a lecture on "Challenges and Opportunities in VLSI" as a keynote speaker. The session provided the insights required about the carrier opportunities in the field of VLSI.

Afternoon session, resource person Ms. K.Shiva Prasanna delivered about " Basic IP Core". In this session, the need and use of IP Core for designing digital logic circuits and their basic implementation using Xilinx Vivado was demonstrated.



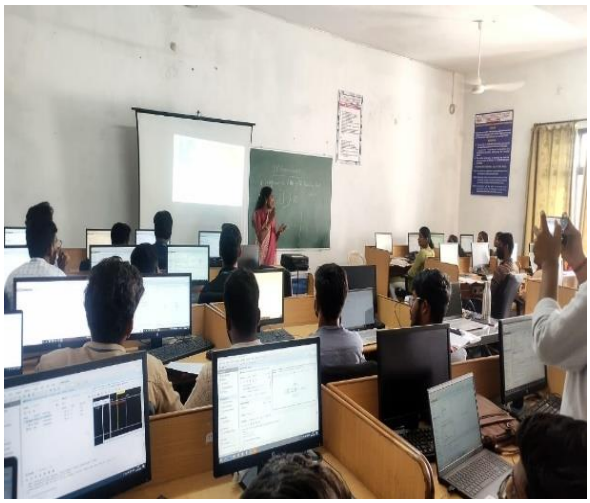


Day-2

A complete day, was handled by Dr.T.Rajasekhar as the resource person on "FPGA Implementation of 64 bit ALU with Artix-7 and Zynq". A hands-on design, implementation and verification of 64-bit ALU was designed using Verilog HDL in Vivado EDA tool. Further, advanced Artix-7 and Zynq FPGA development boards were used for the physical realization of 64-bit ALU. Performances such as area, power and static timing analysis were evaluated during the session.

Day-3

A complete day was handled by the resource person Ms. N.Lavanya and delivered about " Advanced IP Core in VLSI Design". Here, implementation of digital circuits such as adders, subtractors, multiplexers in FPGA boards was demonstrated using advanced options Xilinx Vivado.



Day-4

In morning session, resource person Ms. V.V.Nandini delivered a practical session on " Introduction to Cadence Virtuoso Design Flow ". A hands-on basic design flow of logic gate with schematic and its verification using Cadence was demonstrated.

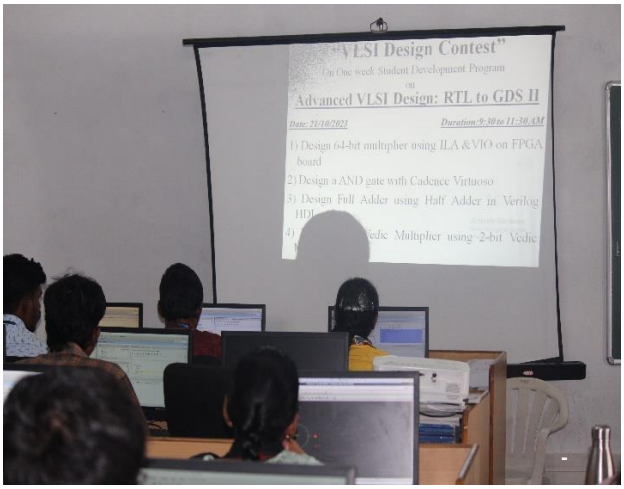
Afternoon session, Mr. K.Ramesh, delivered a hands-on session "IC Design Using Cadence Virtuoso". Here, logic circuits like NAND, EX-OR gates were schematically designed and verified using Cadence Virtuoso.

Day-5

A complete day, was handled by Dr.B.HariPrasad Naik as the resource person on "Physical IC Design". The session covered about physical layout design process of the basic logic gates. During the physical layout, concepts such as DRC, Extraction and LVS was demonstrated using Cadence Virtuoso.

Day-6

In the morning session, an assessment test entitled as "VLSI Design Contest" was conducted by NIVAG for the student participants. Students have actively participated in the contest and are provided with first and second prize excellence certificates.



Finally, the student development program ended with a valedictory session, in the presence of Director, Dr.C.V.Krishna Reddy and Head of Department, Dr. S.Ravi Chand. Student participants received their certificates from the Director, Dr.C.V.Krishna Reddy.

Student Development Program Participants with HOD, Coordinator and Faculty.

Outcomes Of Student Development Program:

After the completion of student development program. Students are skilled with advanced EDA tools and will be able to:

- Design, Implement and Verify Digital VLSI Circuits using HDLs.
- Synthesize and Realize the Circuits using Artix-7 FPGA and Zynq-7000 SoC.
- Design and Verify the Logic Circuits using the IP Cores in FPGA.
- Full-custom design of Integrated Circuits using EDA tools.

Coordinator **HOD-ECE**